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UNITED STATES PATENT APPLICATION

OF

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FOR

IN-PLANE SWITCHING MODE LIQUID CRYSTAL DISPLAY DEVICE AND METHOD FOR MANUFACTURING THE SAME

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[0001] This application claims the benefit of Korean Patent Application No. 2000-81949, filed on December 26, 2000, the entirety of which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

Field of the invention

[0002] The present invention relates to a display device, and more particularly, to an in-plane switching mode liquid crystal display (LCD) device and a method for manufacturing the same.

Background of the Related Art

[0003] An in-plane switching mode LCD device is an LCD device having a wide viewing angle, which has been developed for solving a problem of having a narrow viewing angle in a Twisted Nematic LCD device. In the in-plane switching mode LCD device, common and pixel electrodes are formed on one substrate, and liquid crystals are driven by a horizontal electric field generated between the common and pixel electrodes, so that a viewing angle in the in-plane switching mode LCD device is wider than a viewing angle in the Twisted Nematic LCD device.

[0004] A related art LCD device structure and a method for manufacturing the same will be described with reference to the accompanying drawings.

[0005] FIG. 1A is a structural plan view illustrating a structure of the related art in-plane switching mode LCD device. FIG. 1B is a plan view taken along line I-I' of FIG. 1A.

[0006] As shown in FIG. 1A, the related art in-plane switching mode LCD device includes gate line 211 and data line 212 arranged on an insulating substrate (not shown) to define a pixel region, a common line 213 arranged within the pixel region in parallel with the gate line 211, a thin film transistor formed at a crossing point between the gate line 211 and the data line 212, a pixel electrode 208 arranged within the pixel region in parallel with the

data line 212 and connected with a drain electrode of the thin film transistor, and a common electrode 210 arranged within the pixel region in parallel with the data line 212 and extending from the common line 213.

[0007] The thin film transistor will be described in detail with reference to FIG. 1B. A gate electrode 202 is formed on an insulating substrate 201, and a gate insulating film 203 is formed on the surface of the insulating substrate 201 including the gate electrode 202. Then, a semiconductor layer 204 is formed like an island on the gate insulating film 203 above the gate electrode 202, and an ohmic contact layer 205 is formed on both sides of the gate electrode 202 on the semiconductor layer 204. Source electrode 206 and drain electrode 207 are formed at both sides of the gate electrode 202 above the semiconductor layer 204. An ohmic contact layer 205 is formed between the source and drain electrodes 206 and 207 and the semiconductor layer 204. A pixel electrode 208 is formed on the drain electrode 207 and the gate insulating film 203. A passivation film 209 is deposited on the gate insulating film on which the pixel electrode 208 is formed, and a common electrode 210 is formed on the passivation film 209.

[0008] Generally, in the related art LCD device shown in FIG. 1B, the gate insulating film 203 and the passivation film 209 may consist of a silicon nitride film (SiN_x). The gate electrode 202 may consist of conductive materials such as copper (Cu), titanium (Ti), and chromium (Cr). The source electrode 206 and the drain electrode 207 may consist of chromium (Cr) in taking into consideration of the etching selectivity with a transparent electrode.

[0009] A method for manufacturing the related art in-plane switching mode LCD device will now be described with reference to FIG. 2A to FIG. 2E.

[0010] FIG. 2A to FIG. 2E are plan views illustrating process steps for manufacturing the related art in-plane switching mode LCD device.

[0011] As shown in FIG. 2A, gate line materials and conductive metal materials, are deposited on the insulating substrate 201 by a process such as sputtering. Then, the gate electrode 202 is formed by a patterning process such as photolithography. The gate insulating film 203 consisting of a silicon oxide film or a silicon nitride film, the semiconductor layer 204 of amorphous silicon, and the ohmic contact layer 205 of amorphous silicon containing n-type dopant, are deposited by a process such as plasma enhanced chemical vapor deposition (PECVD).

[0012] As shown in FIG. 2B, the semiconductor layer 204 and the ohmic contact layer 205 formed on the gate insulating film 203, are selectively patterned.

[0013] As shown in FIG. 2C, a data line material, a conductive metal material such as chromium (Cr), is deposited on the ohmic contact layer 205 by a sputtering process, and the source electrode 206 and the drain electrode 207 are formed by a patterning process such as photolithography, so that the thin film transistor is formed.

[0014] As shown in FIG. 2D, the pixel electrode 208 is formed on the drain electrode 207.

[0015] As shown in FIG. 2E, the passivation film 209 is deposited on the substrate, on which the above layers are deposited, by a plasma enhanced chemical vapor deposition (PECVD) process. The transparent common electrode 210 is formed on the passivation layer 209 using a conductive material such as indium tin oxide (ITO). Therefore, the manufacturing process steps of the related art LCD device are completed.

[0016] However, there are following problems in the related art in-plane switching mode LCD device.

[0017] First, the pixel electrode occupies space within the pixel region and so, an aperture ratio is reduced by an area occupied by the pixel electrode.

[0018] The pixel electrode connected with the drain electrode can be formed as the transparent electrode for solving the problem of a decrease in the aperture ratio. However, if etching selectivity between the transparent electrode and the drain electrode is not considered, the drain electrode may be etched during patterning of the transparent electrode. Therefore, reliability of the device may be degraded.

[0019] Furthermore, if the drain electrode material is selected taking into consideration the etching selectivity ratio between the transparent electrode and the drain electrode, chromium is the most appropriate material for the drain electrode.

[0020] But, since chromium has low electricity conductivity, and especially affects resolution, there are limitations in implementing the in-plane switching mode LCD device having high resolution and a large size.

SUMMARY OF THE INVENTION

[0021] Accordingly, the present invention is directed to an in-plane switching mode LCD device and a method for manufacturing the same which substantially obviates one or more problems due to limitations and disadvantages of the related art.

[0022] An advantage of the present invention is to provide an in-plane switching mode LCD device and a method for manufacturing the same that are applicable to an LCD device having high resolution and a large size by improving brightness and aperture ratio without an additional mask.

[0023] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0024] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the in-plane switching mode liquid crystal display device comprises a thin film transistor within a pixel region defined by a plurality of gate lines and data lines; and buffer layer is interposed between a gate electrode and source and drain electrodes of the thin film transistor. The active region includes a gate electrode on an insulating substrate; a gate insulating film on an entire surface of the insulating substrate including the gate electrode; a semiconductor layer and an ohmic contact layer on the gate insulating film; a buffer layer on the ohmic contact layer to cover the semiconductor layer and the ohmic contact layer; source and drain electrodes on the buffer layer; a transparent conductive film for a pixel electrode connected with the drain electrode; a passivation film on the pixel electrode; and a common electrode on the passivation film.

[0025] In another aspect of the present invention, a method for manufacturing the in-plane switching mode LCD device includes selectively depositing a buffer layer on the insulating substrate deposited on the gate electrode, the gate insulating film, the semiconductor layer, and the ohmic contact layer; patterning the buffer layer; forming the transparent conductive film for the pixel electrode through the gate insulating film and the buffer layer; and forming the source and drain electrodes to connect with the transparent conductive film for the pixel electrode.

[0026] In the in-plane switching mode LCD device according to the present invention, the buffer layer is formed on the ohmic contact layer, so that the etching selectivity between the drain electrode and the transparent conductive film is improved and it is possible to prevent the drain electrode from chemically reacting with the ohmic contact layer.

[0027] It is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention.

[0029] In the drawings:

[0030] FIG. 1A is a plan view illustrating a structure of a related art in-plane switching mode LCD device;

[0031] FIG. 1B is a plan view taken along line I-I' of FIG. 1A;

[0032] FIG. 2A to FIG. 2E are sectional views illustrating manufacturing process steps in accordance with the related art in-plane switching mode LCD device;

[0033] FIG. 3 is a sectional view illustrating a structure of an in-plane switching mode LCD device in accordance with the present invention; and

[0034] FIG. 4A to FIG. 4E are sectional views illustrating manufacturing process steps of the in-plane switching mode LCD device in accordance with the present invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0035] Reference will now be made in detail to an embodiment of the present invention, examples of which are illustrated in the accompanying drawings.

[0036] Since a plan structure of an LCD device according to the present invention is the same as a structure of a related art LCD device, the plan structure of the LCD device according to the present invention will be described with reference to the related art plan view.

[0037] FIG. 3 is a sectional view illustrating a structure of an in-plane switching mode LCD device in accordance with the present invention, taken along line I-I' of FIG. 1A. As shown in FIG. 3, the in-plane switching mode LCD device according to the present invention includes an insulating substrate 401; a gate electrode 402 formed on the insulating substrate 401; a gate insulating film 403 formed on the insulating substrate 401 including the gate electrode 402; a semiconductor layer 404, an ohmic contact layer 405 and a buffer layer 406 deposited on the gate insulating film 403 at an upper portion of the gate electrode 402; a transparent pixel electrode 407 connected with the buffer layer 406; source electrode 408 and drain electrode 409 formed on the buffer layer 406; a passivation layer 410 formed on an entire surface of the insulating substrate 401 including the source electrode 408 and drain electrode 409; and a common electrode 411 formed on the passivation layer 410.

[0038] The gate electrode 402 is formed of a low resistance metal such as aluminum (Al), copper (Cu), and silver (Ag).

[0039] The gate insulating film 403 is formed of a silicon nitride film (SiN_x), or a silicon oxide film (SiO_x) and the buffer layer 406 is generally formed of metal such as titanium (Ti).

[0040] As the buffer layer is formed, it is possible to prevent low resistance metals used as the source and drain electrodes from chemically reacting with the ohmic contact layer, and an etching selectivity between the source and drain electrodes and the transparent pixel electrode is improved.

[0041] The manufacturing process steps of the in-plane switching mode LCD device will be described in more detail with reference to FIG. 4A to FIG. 4E.

[0042] As shown in FIG. 4A, one of the low resistance metals such as aluminum (Al), copper (Cu), and silver (Ag) is deposited on the insulating substrate 401 by a sputtering process, and then the gate electrode 402 is formed by a patterning process using

photolithography. The gate insulating film 403 comprising a silicon nitride film or a silicon oxide film is formed on the insulating substrate 401 including the gate electrode 402. The semiconductor layer 404, the ohmic contact layer 405, and the buffer layer 406 of titanium are formed on the gate insulating film 403 by a PECVD process. At this time, the presence of the buffer layer 406 makes it possible to prevent the ohmic contact layer from chemically reacting with a drain electrode, which will be formed.

[0043] As shown in FIG. 4B, the semiconductor layer 404, the ohmic contact layer 405 and the buffer layer 406 of titanium, which are formed on the gate insulating film 403, are patterned. Then, as shown in FIG. 4C, the transparent conductive film for the pixel electrode, such as ITO, is formed on the buffer layer 406 by a sputtering process, and is patterned so that a transparent electrode 407 is formed.

[0044] As shown in FIG. 4D, the source and drain electrodes 408 and 409 are formed of one of aforementioned low resistance metals to connect with the transparent electrode 407 for the pixel electrode on the buffer layer 406.

[0045] As shown in FIG. 4E, the passivation layer 410 is deposited on the entire surface of the insulating substrate 401 including the source and drain electrodes 408 and 409, and then the common electrode 411 is formed on the passivation layer 410.

[0046] Afterwards, a liquid crystal layer is formed between the insulating substrate 401 and an opposing substrate provided with a color-filter and a black matrix (not shown), so that the manufacturing process steps of the in-plane switching mode LCD device according to the present invention are completed.

[0047] As has been explained, the in-plane switching mode LCD device and the method for manufacturing the same according to the present invention have the following advantages.

[0048] In the in-plane switching mode LCD device according to the present invention, brightness and aperture ratio can be improved without an additional mask. Also, the buffer layer comprising titanium (Ti) is deposited on the ohmic contact layer, so that the etching selectivity between the source and drain electrodes and the transparent conductive film is improved, and the buffer layer makes it possible to prevent a chemical reaction between the source and drain electrodes and the ohmic contact layer. Accordingly, the low resistance materials such as aluminum (Al), copper (Cu) and silver (Ag), can be used as the source and drain electrodes, so that the in-plane switching mode LCD device is applicable to the LCD device having fineness and a large size.

[0049] It will be apparent to those skilled in the art that various modifications and variation can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.